REMARKS

In response to the Office Action dated 15 November 2004, the applicants request reconsideration of the above-identified application in view of the following remarks. Claims 1-30 are pending in the application. Claims 1-19 and 28-30 are rejected, and claims 20-27 are allowed. None of the claims are amended herein.

Allowable Subject Matter

The Office Action indicated that claims 20-27 are allowed.

Rejection of Claims Under §112

Claim 1 was rejected under 35 USC § 112, first paragraph. The applicants respectfully traverse.

Claim 1 was rejected based on the objection to claim 6. Claim 6 is supported by Figures 1 and 2, the description, and by the fact that claim 6 itself was a part of the original disclosure. Figure 1 shows the processor 106 coupled to the synchronization circuit 112. The synchronization circuit 112 is shown in detail in Figure 2 having a node 202 to receive the AREADY signal and a node 214, and both nodes 202 and 214 are to be coupled to other circuits such as the processor 106. The description states that the AREADY signal can be asserted by the processor 106. [1] One skilled in the art would understand how the processor 106 is coupled to the synchronization circuit 112 to assert the AREADY signal without undue experimentation.

Rejection of Claims Under §102

Claims 28 and 29 were rejected under 35 USC § 102(e) as being anticipated by Walker (U.S. 6,127,849). The applicants respectfully traverse.

Walker issued on October 3, 2000, which is after the filing date of the present application. The applicants do not admit that Walker is prior art, and reserve the right to swear behind Walker at a later date. However, the applicants believe Walker is distinguishable from the claimed invention.

[1] Specification, page 6, line 18.

Claim 28 recites a method of synchronizing an agent to a bidirectional bus including, among other elements, de-asserting a ready signal to drive a transmission line having a second agent driver present thereon to signify the agent is not ready to communicate on the bidirectional bus and asserting the ready signal to signify the agent is ready to communicate on the bidirectional bus. Claim 29 is dependent on claim 28, and recites further features with respect to claim 28.

Walker relates to a simultaneous bi-directional I/O circuit.[2] Walker shows a transistor-level diagram of an I/O circuit 300 in Figure 3A and describes its operation with respect to a timing diagram in Figure 3B. Other transistor-level diagrams of I/O circuits 500 and 600 are shown in Figures 5 and 6, respectively. Walker describes a data transmitting system 400 in Figure 4A with a timing diagram in Figure 4B.[3] Throughout the description, Walker refers to transistor-level devices that prevent glitches from being latched.

Walker does not discuss de-asserting a ready signal to signify the agent is not ready to communicate or asserting the ready signal to signify the agent is ready to communicate as are recited in independent claim 28.

The applicants respectfully submit that Walker does not show all of the elements recited in claims 28 and 29, and that claims 28 and 29 are in condition for allowance.

Rejections of Claims Under §103

Claims 1-5, 7-11, 13-16, 19, and 30 were rejected under 35 USC § 103(a) as being unpatentable over Walker in view of Cowell (U.S. 5,860,134). The applicants respectfully traverse.

Independent claims 1 and 9 each recite an integrated circuit including, among other elements, a receiver having input hysteresis. Independent claim 14 recites a bidirectional port including, among other elements, a data driver and a synchronization circuit.

[2] Walker, Title.
[3] Walker, column 8, line 47 to column 9, line 65.

Walker was discussed above. Cowell relates to a memory system and describes presence and type detect circuitry 500 for a memory controller 103.[4] The circuitry 500 includes a receiver 507 with hysteresis.[5]

Walker and Cowell, even as combined, do not show a data driver and a synchronization circuit. Therefore, Walker and Cowell do not show all of the features recited in independent claim 14.

Regarding independent claims 1 and 9, Walker describes a data transmitting system 400 with an output buffer 406a and an input buffer 408a.[6]

The MPEP requires a suggestion and a reasonable expectation of success for a rejection under 35 USC § 103:

> "To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations."[7]

The suggestion or motivation to combine references and the reasonable expectation of success must both be found in the prior art.[8]

The Office Action states:

> "it would have been obvious ... to have combined the teachings of Cowell within the system of Walker because it would provide a flexible mechanism for port selections."[9]

The Office Action has not identified prior art as being the source of the above-quoted rationale for combining Walker and Cowell as is required by MPEP 2143.

The Office Action has also not identified a reasonable expectation of success in the prior art as is required by MPEP 2143. The circuits of Walker are shown and described on the transistor level. The Office Action has not specified where the receiver 507 with

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[4] Cowell, column 6, line 31 to column 7, line 25.
[5] Cowell, column 7, lines 4-9.
[6] Walker, column 8, lines 47-65.
[7] MPEP 2143.
[8] MPEP 2143.
[9] Office Action, pages 4-5.

hysteresis from Cowell is to be placed in the circuits of Walker. The Office Action has not shown that such an change at the transistor level of the circuits of Walker would have a reasonable expectation of success.

With regard to other claimed features, the Office Action states:

> "even though the teachings of Walker does not specifically disclose output impedance of the pullup transistor is at least 5 times greater than the output impedance of the pulldown transistor, however one skilled in the art would have understood that they can choose set the number of time being greater to fulfill their need."[10]

The Office Action also states:

> "even though the teachings of Walker does not specifically disclose the IC is the circuit type from the group of processor, memory, however one skilled in the art would have understood that they can choose to implement the design into variety of type of circuits to fulfill their need."[11]

The Office Action has not identified prior art as being the source of the above-quoted rationales for modifying Walker as is required by MPEP 2143.

The applicants respectfully submit that a *prima facie* case of obviousness against claims 1-5, 7-11, 13-16, and 19 has not been established in the Office Action, and that claims 1-5, 7-11, 13-16, and 19 are in condition for allowance.

Claim 30 is dependent on claim 28, and recites further features with respect to claim 28. For reasons analogous to those stated above, and the features in the claims, the applicants respectfully submit that claim 30 is not shown or suggested by Walker and Cowell, and that claim 30 is in condition for allowance.

Claims 12 and 17-18 were rejected under 35 USC § 103(a) as being unpatentable over Walker in view of Cowell and further in view of Oprescu et al. (U.S. 5,325,355, Oprescu). The applicants respectfully traverse.

Claims 12, 17, and 18 each recite a slew rate control circuit. The Office Action also states:

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[10] Office Action, page 5.
[11] Office Action, page 5.

> "Walker and Cowell disclose ... except the teaching of wherein the initialization circuit including a slew rate control circuit."[12]

Oprescu relates to a bus system shown in Figure 1. Oprescu does not show a slew rate control circuit. The Office Action also states:

> "it would have been obvious ... to have combined the teachings of Oprescu et al. within the systems of Walker and Cowell because it would improve the speed of the data transfers."[13]

The Office Action has not identified prior art as being the source of the above-quoted rationale for combining Walker, Cowell, and Oprescu as is required by MPEP 2143.

The applicant respectfully submits that a *prima facie* case of obviousness against claims 12 and 17-18 has not been established in the Office Action, and that claims 12 and 17-18 are in condition for allowance.

[12] Office Action, page 6.
[13] Office Action, page 6.

CONCLUSION

The applicants respectfully submit that all of the pending claims are in condition for allowance, and such action is earnestly solicited. The Examiner is invited to telephone the below-signed attorney at 612-373-6973 to discuss any questions which may remain with respect to the present application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date 15 March 2005

By /Reg/
Robert E. Mates
Reg. No. 35,271

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 15th day of March, 2005.

Amy Moriarty
Name

Signature